




## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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Title of Invention	Symbolic model checking with dynamic model pruning						
Application Number:		10/666619					
Confirmation Number:		6808					
First Named Applicant:		Jin Yang					
Attorney Docket Number:		42P8534C					
Art Unit:		2825					
Examiner:		Annette Thompson					
Search string:		( 5870509 or 6484134 ).pn.					
US Patent Documents							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5870509	1999-02-09	Kita et al.			
S.P.	2	6484134	2002-11-19	Hoskote			
Signature							
Examiner Name				Date			
<i>Sushin Pasikun</i>				3-6-06			

Substitute for Form 1449A/PTO (Modified)				Attorney Docket No.: 42P8534C		Application Number: Unassigned 10-666619	
Sheet 1 of 4				First Named Inventor: Jin Yang		Examiner: Unassigned	
				Filing Date: Herewith		Art Unit: Unassigned	
<b>U.S. PATENT DOCUMENTS</b>							
Exam. Initial*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number	Kind Code <sup>2</sup> (If known)				
S.P.		5,119,318		Paradies et al.	06/02/1992		
S.P.		5,481,717		Gaboury	01/02/1996		
S.P.		5,469,367		Puri et al	11-21-1995		
S.P.		5,491,639		Filkorn	02-13-1996		
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S.P.		6,339,837		Li	01-15-2002		
S.P.		6,341,367		Downing	01/22/2002		
		B1					
Examiner Signature						Date Considered 2/22/06	

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Sheet 2 of 4	Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 42P8534C	Application Number: Unassigned
		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: Herewith	Art Unit: Unassigned

**OTHER ART - NO PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
S.P.		BEREZIN, S. et al, "A Compositional Proof System for the Modal $\mu$ -Calculus and CCS," <i>Technical Report CMU-CS-97-105, Carnegie Mellon University, January 15, 1997</i>	
S.P.		BEREZIN, S. et al, "Model Checking Algorithms for the $\mu$ -Calculus," <i>Technical Report CMU-CS-96-180, Carnegie Mellon University, September 23, 1996</i>	
S.P.		BRADLEY, J. et al, "Compositional BDD Construction: A Lazy Algorithm," <i>Dept. of Computer Science, University of Bristol, April 1998, pages 1-8.</i>	
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S.P.		BRYANT, R. E., "Binary Decision Diagrams & Beyond," <i>Tutorial at ICCAD '95, Carnegie Mellon University, 1995</i>	
S.P.		BURCH, J. R. et al, "Representing Circuits More Efficiently in Symbolic Model Checking," <i>28<sup>th</sup> ACM/IEEE Design Automation Conference, Paper 24.3, 1991, pages 403-407</i>	
S.P.		BURCH, J. R. et al, "Sequential Circuit Verification Using Symbolic Model Checking," <i>2<sup>nd</sup> ACM/IEEE Design Automation Conference, Paper 3.2, 1990, pages 46-51</i>	
S.P.		BURCH, J. R. et al, "Symbolic Model Checking for Sequential Circuit Verification," <i>IEEE Transactions on Computer-Aided Design for Integrated Circuits and Systems, April 1994, pages 401-424</i>	
S.P.		CAMPOS, S., "Real-Time Symbolic Model Checking for Discrete Time Models," <i>Technical Report CMU-CS-94-146, Carnegie Mellon University, Pittsburgh, PA, May 2, 1994</i>	
S.P.		CAMPOS, S., "Symbolic Model Checking in Practice," <i>IEEE Proceedings, XII Symposium on Integrated Circuits and System Design, Oct 2, 1999, pages 98-101.</i>	
S.P.		CHAN, W. et al, "Combining Constraint Solving and Symbolic Model Checking for a Class of Systems with Non-linear Constraints," <i>Computer Aided Verification, 9<sup>th</sup> International Conference, CAV '97 Proceedings (O. Grumberg, Editor), Lecture Notes in Computer Science 1254, pages 316-327, Haifa, Israel, June 1997. Springer-Verlag (Revised in December '98)</i>	
S.P.		CHEN, Y. et al, "PBHD: An Efficient Graph Representation for Floating Point Circuit Verification," <i>Technical Report CMU-CS-97-134, Carnegie Mellon University, May 1997</i>	

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Sheet 3 of 4	First Named Inventor: Jin Yang	Examiner: Unassigned
	Filing Date: Herewith	Art Unit: Unassigned

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SR		CHEUNG, S. et al, "Checking Safety Properties Using Compositional Reachability Analysis," <i>ACM Transactions on Software Engineering and Methodology</i> , Vol. 8, No. 1, January 1999, pages 49-78	
SR		CHIODO, M. et al, "Automatic Compositional Minimization in CTL Model Checking," <i>Proceedings of 1992 IEEE/ACM International Conference on Computer-Aided Design</i> , November, 1992, pages 172-178	
SR		CHOU, C., "The Mathematical Foundation of Symbolic Trajectory Evaluation," <i>International Conference on Computer-Aided Verification(CAV'99)</i> , Trento, Italy, July 1999 pp. 196-207, <i>Proceedings of CAV'99, Lecture Notes in Computer Science #1633</i> (Editors: Nicolas Halbwachs & Doron Peled), Springer-Verlog, 1999	
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SR		CLARKE, E. et al, "Combining Symbolic Computation and Theorem Proving: Some Problems of Ramanujan," <i>Technical Report CMU-CS-94-103, Carnegie Mellon University</i> , January 1994	
SR		CLARKE, E. M. et al, "Formal Methods: State of the Art and Future Directions," <i>ACM Computing Surveys</i> , Vol. 28, No. 4, December 1996, pages 626-643	
SR		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>Proceedings of the 19<sup>th</sup> ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 343-354	
SR		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>ACM Transactions on Programming Languages and Systems</i> , Vol. 16, No. 5, September 1994, pages 1512-1542	
SR		GRUMBERG, O., "Model Checking and Modular Verification," <i>ACM Transactions On Programming Languages and Systems</i> , Vol. 16, No. 3, May 1994, pages 843-871	
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SR		JACKSON, D., "Exploiting Symmetry in the Model Checking of Relational Specifications," <i>Technical Report CMU-CS 94-219, Carnegie Mellon University</i> , December 1994	

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Sheet 4 of 4	First Named Inventor: Jin Yang	Examiner: Unassigned
	Filing Date: Herewith	Art Unit: Unassigned

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Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
S.P.		JAIN, A. et al, "Verifying Nondeterministic Implementations of Determinist Systems," <i>Lecture Notes in Computer Science, Formal Methods in Computer Aided-Design</i> , pp. 109-125, November 1996	
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S.P.		NELSON, K. L. et al, "Formal Verification of a Superscalar Execution Unit," <i>34<sup>th</sup> Design Automation Conference</i> , June 1997	
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S.P.		VELEV, M. N., "Efficient Modeling of Memory Arrays in Symbolic Simulations," <i>Proceedings of Computer-Aided Verification</i> , June 1997	
S.P.		WING, J. M. et al, "A Case Study in Model Checking Software Systems," <i>Technical Report CMU-CS-96-124, Carnegie Mellon University, Pittsburgh, PA</i> , April 1996	
S.P.		YEH, W. et al, "Compositional Reachability Analysis Using Process Algebra," <i>28<sup>th</sup> ACM/IEEE Design Automation Conference</i> , 1991	
S.P.		Zhang Z., "An Approach to Hierarchy Model Checking via Evaluating CTL Hierarchically," <i>IEEE Proceedings of the Fourth Asian Test Symposium</i> , Nov. 24, 1995, pages 45-49.	

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